

Appln No. 09/872,645

Amdt date November 14, 2005

Reply to Office action of September 29, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.-3. Cancelled.

4. (Previously presented) An encoder, comprising:
a state machine configured to generate a plurality of state bits, and
an interface configured to couple an input relating to one of the state bits into the state machine during a time period,

wherein the interface is configured to couple an input signal into the state machine during a second time period, and couple a complement of said one of the state bits into the state machine during the time period.

5.-12. Cancelled.

13. (Previously presented) An encoder, comprising:
state generation means for generating a plurality of state bits, and
interface means for coupling an input relating to one of the state bits into the state generation means during a time period,

wherein the interface means is configured to couple an input signal into the state generation means during a second time period, and coupled a complement of said one of the state bits into the state machine during the time period.

14.-21. Cancelled.

Appln No. 09/872,645

Amdt date November 14, 2005

Reply to Office action of September 29, 2005

22. (Currently amended) A transmitter, comprising:
an encoder having,
a state machine configured to generate a
plurality of state bits, and
an interface configured to couple an input
relating to one of the state bits into the state machine during
a time period; and
an RF stage coupled to the encoder;
wherein the RF stage and the encoder are each an integral
part of the transmitter and ~~The encoder of claim 19~~ wherein the
interface is configured to couple an input signal into the state
machine during a second time period, and coupled a complement of
said one of the state bits into the state machine during the
time period.

23.-27. Cancelled.

28. (Currently amended) A transmitter, comprising:
an encoder having,
a state machine configured to generate a
plurality of state bits, and
an interface configured to couple an input
relating to one of the state bits into the state machine during
a time period;
an RF stage coupled to the encoder; and
~~The transmitter of claim 19 further comprising a~~
transmit control unit coupled to the encoder, the transmit
control unit being configured to control the interface[.];
wherein the RF stage and the encoder are each an integral
part of the transmitter.

Appln No. 09/872,645

Amdt date November 14, 2005

Reply to Office action of September 29, 2005

29. (Currently amended) The transmitter of claim 28 further comprising a preamble generator coupled to the transmit control ~~legie~~ unit.

30. (Currently amended) The transmitter of claim 28 further comprising a CRC generator coupled to the transmit control ~~legie~~ unit.

31.-33. Cancelled.

34. (Currently amended) A transmitter, comprising:
an encoder having,
state generation means for generating a plurality
of state bits, and
interface means for coupling an input relating to
one of the state bits into the state generation means during a
time period; and
an RF stage coupled to the encoder;
wherein the RF stage and the encoder are each an integral
part of the transmitter and ~~The transmitter of claim 31~~ wherein
the interface means [[is]] are configured to couple an input
signal into the state generation means during a second time
period, and couple a compliment of said one of the state bits
into the state machine during the time period.

35.-39. Cancelled.

40. (Currently amended) A transmitter, comprising:
an encoder having,
state generation means for generating a plurality
of state bits, and

Appln No. 09/872,645

Amdt date November 14, 2005

Reply to Office action of September 29, 2005

interface means for coupling an input relating to one of the state bits into the state generation means during a time period;

an RF stage coupled to the encoder; and

~~The transmitter of claim 31 further comprising~~
transmit control means for controlling the interface means to couple the input relating to one of the state bits into the state generation means during the time period[.];

wherein the RF stage and the encoder are each an integral part of the transmitter.

41. (Original) The transmitter of claim 40 further comprising means for generating a preamble coupled to the transmit control means.

42. (Original) The transmitter of claim 40 further comprising means for generating a CRC coupled to the transmit control means.

43.-44. Cancelled.

45. (Previously presented) An encoder, comprising:
a state machine configured to generate a state, and
an interface configured to serially couple an input relating to a binary representation of the state into the state machine during a time period,

wherein the interface is configured to serially couple a plurality of input signals into the state machine during a second time period, and serially couple a compliment of the binary representation of the state at the end of the second period into the state machine during the time period.

Appln No. 09/872,645

Amdt date November 14, 2005

Reply to Office action of September 29, 2005

46.-51. Cancelled.

52. (Previously presented) An encoder, comprising:
state generation means for generating a state, and
interface means for serially coupling an input
relating to a binary representation of the state into the state
machine during a time period,

wherein the interface comprises a switch configured to
serially couple the input signals into the state generation
means during the second time period, and serially couple a
compliment of the binary representation of the state at the end
of the second period into the state generation means during the
time period.

53.-57. Cancelled.

58. (Previously presented) A method of generating a
signal, comprising:

generating a payload as a function of a state machine
output,

generating a tail as a function a binary
representation of the state machine output at the end of the
payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of
state bits, the tail generation comprising serially feeding a
compliment for each of the state bits for the binary

Appln No. 09/872,645

Amdt date November 14, 2005

Reply to Office action of September 29, 2005

representation of the state machine output at the end of the payload generation into the state machine.

59. (Previously presented) A method of generating a signal, comprising:

generating a payload as a function of a state machine output,

generating a tail as a function of a binary representation of the state machine output at the end of the payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of first state bits having a most significant bit, the tail generation comprising feeding the most significant bit of the first state bits into the state machine during a first clock cycle to generate a second plurality of state bits having a most significant bit, and feeding the most significant bit of the second state bits into the state machine during a second clock cycle.

60. (Original) The method of claim 59 wherein the first state bits further comprise a least significant bit, and wherein the most significant bit of the second state bits is the least significant bit of the first state bits.

61. (Previously presented) A method of generating a signal, comprising:

generating a payload as a function of a state machine output,

Appln No. 09/872,645

Amdt date November 14, 2005

Reply to Office action of September 29, 2005

generating a tail as a function of a binary representation of the state machine output at the end of the payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of first state bits having a most significant bit, the tail generation comprising feeding a compliment of the most significant bit of the first state bits into the state machine during a first clock cycle to generate a second plurality of state bits having a most significant bit, and feeding a compliment of the most significant bit of the second state bits into the state machine during a second clock cycle.

62. (Original) The method of claim 61 wherein the first state bits further comprise a least significant bit, and wherein the most significant bit of the second state bits is the least significant bit of the first state bits.